

School of Engineering

Department of Electrical and Computer Engineering

**Capstone Project Proposal**

**Project Number**:

**Project Title**:

**Project term**: Fall 2017

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This project seeks to create a custom hardware graphics accelerator that uses sprite rendering to generate a VGA display running at 60 frames per second. The functionality of the accelerator is then proven by combining it with a Microcontroller in order to create a full-functioning gaming system. By creating a gaming system and programming a sample game, the system is a proof-of-concept that validates the functionality of the graphics hardware and provides a sample test-case for those interested in leveraging the design in future systems.

This project seeks to demonstrate and expand the knowledge of the partners, as well as to create a viable prototype of a consumer electronics product. Creation of the system demonstrates a high level understanding of topics such as Computer Architecture, Embedded Software Development, and Digital Design, as well as System Design and Testing, all while creating an entertaining product that is accessible to a wide audience.

The most viable options for developing this project include using only a Microcontroller, using only an FPGA, or utilizing both. Utilizing only a Microcontroller would require sacrificing video quality and/or frame rate due to the amount of repetitive instructions necessary for moving large amounts of memory in order to produce the display. Utilizing only the FPGA would limit our ability to perform complex operations necessary for the game control logic. An option would be to include a soft-core processor in our architecture, however, this processor would run slower than a dedicated hard processor. Utilizing both the FPGA and the Microcontroller allows us to attempt to make the most of the advantages of each one.

By taking advantage of the best capabilities of each device (the FPGA and the Microcontroller), we can create an embedded system capable of generating high detail, high speed graphics while running complex control logic to create an interactive experience. All of the heavy lifting for the display generation and processing is done by the hardware acceleration in the FPGA fabric, while the control logic for the physics, player interaction, and game logic is handled by the microcontroller. A bus communication interface allows the Microcontroller to send commands to the hardware accelerator and a second communication interface allows the accelerator to read from the sprite memory controlled by the processor.  In this way, we can achieve a high performance, low cost solution that does not require compromises in the design.